IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.:	10/667870	Confirmation No.:	1168
Applicant:	Coppola	Examiner:	Fields,Courtney D.
Filed:	22-SEP-2003	Art Unit:	2137

Docket No.: TI-34641
Customer No.: 23494
For: High-Speed, Accurate Trimming For Electronically Trimmed VCO

APPELLANTS' BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellants respectfully present this brief in support of their appeal of the final rejection of the claims in this case. The Notice of Appeal was filed on February 28, 2006. A fee for filing this brief in support the appeal is submitted herewith.

i. Real party in interest

The real party in interest in this application is Texas Instruments Incorporated.

ii. Related Appeals and Interferences

The undersigned is aware of no appeals or interferences which will directly affect or have a bearing on, or be directly affected by, the Board's decision in this appeal.

iii. Status of claims

Claims 1 through 12 were finally rejected in the Office Action of September 29, 2006 and are the subject of the present appeal.

iv. Status of amendments

A response under CFR 1.116 was submitted on January 29, 2007. No amendments were made in the response.

v. *Summary of claimed subject matter*

A. ***Overview***

The inventive claimed subject matter relates to a tuning circuit using a voltage controlled oscillator (VCO). The VCO generates a first clock signal using an inductive element, a variable capacitive element, and a bank of switched capacitors. A frequency divider generates a second clock signal responsive to the first clock signal and a selected divisor. Responsive to a frequency difference between the second clock signal and a reference signal, frequency control circuitry adjusts a control voltage to the variable capacitive element in order to oscillate the first clock signal at a desired frequency.

The output frequency can be varied by changing the divisor. When a new desired frequency is specified by a change in the divisor, logic circuitry calibrates the VCO to operate in a frequency range inclusive of the new desired frequency. To do this, the logic circuitry performs a coarse search by operating the VCO at a single predetermined control voltage for various capacitive settings of the bank to determine an initial control word for configuring the bank. After the coarse search, the initial control word is tested to determine whether the initial control word should be used to generate the first clock signal at the new desired frequency or whether the initial control word should be changed to an adjacent control word to generate the first clock signal at the new desired frequency.

B. ***Relating Overview to Independent Claims***

Independent claims 1 and 7 are pending in this appeal. Each is set forth below with reference numbers of examples, in parenthesis, and with reference to support in the text and drawings of the Specification and consistent with the Overview provided above.

1. Claim 1

Claim 1 is directed to a tuning circuit (50) including a voltage controlled oscillator (56) for generating a first clock signal (f_{VCO})[1]. The VCO (56) includes an inductive element (12), a variable capacitive element (14) coupled to the inductive element and a bank (21) of switched capacitors (22) coupled to the inductive element and the variable capacitive element[2]. A frequency divider (54) generates a second clock signal responsive to the first clock signal and a selected divisor.[3] Frequency control circuitry (52) adjusts a control voltage to the variable capacitive element responsive to a frequency difference between the second clock signal and a reference signal to oscillate the first clock signal at a desired frequency.[4] Logic circuitry (66) calibrates the VCO (56) to a frequency range inclusive of a new desired frequency responsive to a change in the divisor by performing a coarse search by operating the voltage controlled oscillator at a single predetermined control voltage for various capacitive settings of the bank to determine an initial control word for configuring the bank (step 30) and testing the initial control word to determine whether the initial control word should be used to generate the first clock signal at the new desired frequency or whether the initial control word should be changed to an adjacent control word to generate the first clock signal at the new desired frequency (steps 32-44).[5]

This aspect of the invention provides significant advantages over the prior art. The coarse search provides an initial control word near the optimum control word. From the range provided by the initial control word, it can be quickly determined to whether to change the initial control word to an adjacent control word to reach an optimum range. This results in fast and accurate switching.

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[1] Figure 8, Specification paragraphs [0042] – [0044].
[2] Figure 3, Specification paragraphs [0029] – [0031].
[3] Figure 8, Specification paragraphs [0042] – [0043].
[4] Figure 8, Specification paragraph [0044].
[5] Figures 7 and 8, Specification paragraphs [0039] – [0041], [0045] – [0046].

2. Claim 7

Claim 7 is a method of calibrating a voltage controlled oscillator (56) for generating a first clock signal (f_{VCO})[6], where the VCO has an LC tank (20) with an inductive element (12), a variable capacitive element (14) coupled to the inductive element, where the capacitance of the variable capacitive element is controlled by a control voltage, and a bank (21) of switched capacitors (22) coupled to the inductive element and the variable capacitive element. [7] An initial control word is determined to configure the bank using a search in which the voltage controlled oscillator is operated at a single predetermined control voltage for various capacitive settings of the bank and the initial control word is tested to determine whether the frequency range produced by the initial control word should be used to generate the first clock signal at the new desired frequency or whether the initial control word should be changed to an adjacent control word to generate the first clock signal at the new desired frequency. [8]

Claim 7 provides the same benefits stated above for claim 1.

C. Relating Overview to Dependent Claims

1. Claims 3 and 9

Claims 3 and 9 are dependent upon claims 1 and 7, respectively. These claims are related to testing the initial control word by comparing the desired frequency to upper and lower bounds of a frequency range for the voltage controlled oscillator while configured according to the initial control word.[9]

2. Claims 4 and 10

Claims 4 and 10 are dependent upon claims 3 and 9, respectively. In these claims, the initial control word is determined using fast comparisons between an actual

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[6] Figure 8, Specification paragraphs [0042] – [0044].
[7] Figure 3, Specification paragraphs [0029] – [0031].
[8] Figures 7 and 8, Specification paragraphs [0039] – [0041], [0045] – [0046].
[9] Figure 7, paragraphs [0040] – [0041].

frequency at the predetermined control voltage and the desired frequency and whether the initial control word should remain the same is determined by using more precise comparisons between the actual frequency and the desired frequency.[10]

3. Claims 5 and 11

Claims 5 and 11 are dependent upon claims 1 and 7, respectively. In these claims, the initial control word is tested by determining whether the difference between the desired frequency and an actual frequency for the voltage controlled oscillator, while configured according to the initial control word, is within a predetermined threshold.[11]

[10] Specification, paragraph [0048].
[11] Figure 11, Specification paragraphs [0053] – [0054].

vi. Grounds of rejection to be reviewed on appeal

A. Rejections Under 35 U.S.C. § 103

The Examiner has rejected claims 1-12 under 35 U.S.C. §103(a) as being unpatentable over U.S. Pub. No. 2002/0075080 to Nelson in view of U.S. Pat. No. 6,323,736 to Jansson.

With regard to Claims 1 and 7, the Examiner states that Nelson shows all of the elements of the invention, including a tuning circuit (300) comprising a VCO (24), a frequency divider (38), frequency control circuitry (34), and logic circuitry (32), citing paragraphs [0021] – [0024] of Nelson, with the exception that Nelson does not show that the VCO is a digitally controlled VCO. Jansson is cited to show an LC tank VCO with a digitally controlled bank of capacitors, which is used in a PLL for tuning a desired oscillation frequency digitally, so that it can provide self calibration as shown by Jansson.[12] The Examiner states that testing of the initial control word is shown in Nelson by reference to U.S. Pat. No. 5, 942,949 to Wilson (hereinafter "Wilson"), which is cited in the Nelson reference at paragraph [0020].[13]

With regard to claims 3 and 9, the Examiner states that Nelson discloses the logic circuitry (state machine 22) and tests and initial control word ("L", at paragraph [0018]) by comparing the desired frequency to upper (max) and lower (min) bounds of a frequency range for the VCO while configured to the initial control word.[14] The Examiner further states that Wilson shows calibration for Max and Min as a result of driving V_{LF} to the positive and negative supply rails, citing column 4, lines 3-12 of Wilson.[15]

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[12] Office Action of January 31, 2006, pages 2-3.
[13] Office Action of September 29, 2006, page 3.
[14] Office Action of January 31, 2006, page 4.
[15] Office Action of September 29, 2006, page 3.

With regard to claims 4 and 10, the Examiner states that Nelson discloses fast comparisons when SW2 is closed and more precise comparisons take place with SW1 is closed, citing paragraph [0022].[16]

With regard to claims 5 and 11, the Examiner states that Nelson discloses testing the initial control word (L) within a predetermined threshold, citing "max" and "min" of paragraph [0018].[17]

[16] Office Action of January 31, 2006, page 4.
[17] Office Action of January 31, 2006, page 4.

vii. Argument

Appellants respectfully submit that the final rejection fails to meet the obviousness standard. Instead, the teachings of the applied prior art, properly interpreted, fall short of showing each and every element of the claims when taken in combination and there is no suggestion from the prior art to modify those teachings in such a manner as to reach the claims on appeal in this case. Further, Applicants respectfully submit that the Wilson reference is improperly used in this case, because it has not been cited by the Examiner.

A. Independent Claims 1 and 7

The present invention, as defined by claims 1 and 7, include (in part) circuitry or steps for:

> performing a coarse search by operating the voltage controlled oscillator at a single predetermined control voltage for various capacitive settings of the bank to determine an initial control word for configuring the bank; and
>
> testing the initial control word to determine whether the initial control word should be used to generate the first clock signal at the new desired frequency or whether the initial control word should be changed to an adjacent control word to generate the first clock signal at the new desired frequency.

The logic circuitry described in the present specification thus performs two functions to accurately and quickly calibrate a VCO. First, a coarse search is performed at a single control voltage at various capacitive settings of the bank. This yields an initial control word. The initial control word is then tested to determine whether it should be used to generate the first clock signal at the new desired frequency, or if the initial control word should be changed to an adjacent control word to generate the first clock signal to generate the first clock signal at the new desired frequency.

The Nelson reference does not provide any teaching of testing the initial control word to determine whether the initial control word should be used to generate the first

clock signal at the new desired frequency, or if the initial control word should be changed to an adjacent control word to generate the first clock signal to generate the first clock signal at the new desired frequency. On the contrary, Nelson explicitly states in paragraph [0024] that:

> By purposefully selecting VCO center frequency control signals, L, state machine 32 may identify the two VCO operating curves that have center frequencies just above and just below the frequency of the input signal R. *Either one of these two operating curves may be selected for use during normal PLL operations*.

Accordingly, *no* testing is done after the initial search, and there is no determination made as to whether a control word adjacent to the initial control word would be better for generating the first clock signal at the new desired frequency.

In response to the argument set forth above, The Examiner states that:

> For clarification, the calibration is described in the supporting document US Pat. No. 5,942,949 as stated in paragraph [0020]. As described in Column 3, line 55 - Column 4, line 59 of US Pat. No. 5,942,949, state machine 316 performs a linear search algorithm or a binary search algorithm and further states that "each digital control input value N needs to be maintained to test each of the VCO operating curves in the search sequence".

The claims of the present application have not been formally rejected over the Wilson patent, U.S. Pat. No. 5,942,949; the Examiner is treating the Wilson patent as if it were part of the specification of the Nelson reference. The Wilson patent is not incorporated by reference in the Nelson reference, nor is it used by the Nelson reference to describe how a VCO curve is selected. In the Nelson reference, Wilson is simply used as an example of a self trimming PLL circuit which does not address automatic self-calibration of VCO gain. Applicants believe that it is improper to reject claims in the present application based on a disclosure which was not cited as a reference prior to the final rejection, simply because the reference is cited in the Nelson publication as prior

art. Had the Wilson patent been formally cited in a rejection under C.F.R. 103 in the Office Action of September 29, 2006, the rejection could not properly have been made final.

With regard to the merits of the rejection using the Wilson patent as a reference, Applicants disagree with the Examiner's assertions. Similar to Nelson, Wilson states:

> The desired frequency of the VCO output signal F_{OSC} is the frequency of the input signal F_{IN} (ignoring for the time being any frequency multiplication or division resulting from dividers 310 or 312). By purposefully selecting digital control input values N, state machine 316 can eventually identify the two VCO operating curves that have center frequencies just above and just below the frequency of the input signal F_{IN}. *Either one of these two operating curves can then be selected for use during normal PLL operations.* In one embodiment, state machine 316 performs a linear search algorithm in which the values for the digital control input N are selected linearly starting at one end of the range of possible values (e.g., 0) and proceeding towards the other end of the range until the quiescent loop-filter voltage V_{LF} flips from one side (e.g., ground) to the other (e.g., V_{DD}). In an alternative embodiment, state machine 316 performs a binary search algorithm in which each new digital control input value is selected midway between two previously selected values that yielded opposing quiescent loop-filter voltages, until two consecutive digital control values are found that yield opposing quiescent loop-filter voltages. [Emphasis added]

Like Nelson, the Wilson reference does not provide any teaching of testing *at the initial control word* to determine whether it should be used to generate the first clock signal at the new desired frequency, or if the initial control word should be changed to an adjacent control word to generate the first clock signal to generate the first clock signal at the new desired frequency. Wilson simply finds two adjacent VCO operating curves that have center frequencies above and below the frequency of the input signal F_{IN} and selects one of the operating curves.

Accordingly, even with the Wilson reference, *no* testing is done *after the initial search*, and there is *no determination made as to whether a control word adjacent to the initial control word would be better for generating the first clock signal at the new desired frequency.*

Hence, Appellant submits that claim 1 and 7 are novel and unobvious over the prior art.

B. Dependent Claims 3 and 9

The Examiner states that Nelson teaches the function of testing an initial control word by comparing the frequency to upper (max) and lower (min) bounds of a frequency range for the VCO while configured to the initial control word, referring to paragraph [0018] of Nelson. This paragraph has no such teaching – it is simply a description of the exemplary operating curves shown in Figure 2A, and contains no teaching of testing at the endpoints of the curves, or anywhere else on the curves.

With regard to the Examiner's reliance upon Wilson to show the subject matter of these claims, Applicants believe that the Examiner has misinterpreted the teaching of Wilson. In Wilson, V_{REF} is applied to the voltage input of VCO 308, V_{REF} being at the nominal center of the range of input voltages. This is to generate a frequency F_{OCS} at the center of the frequency range. The sentence recited by the Examiner states that the charge pump 304 will eventually drive the loop-filter voltage V_{LF} either to ground or V_{DD} depending upon whether the frequency of the feedback signal is greater or less than the frequency of the input signal F_{IN}. Depending upon which rail V_{LF} converges on, it can be determined whether the *center frequency* of the VCO curve was higher or lower than F_{IN}. There is, however, no comparison between the desired frequency to *upper* and *lower* bounds of a frequency range for the voltage controlled oscillator while configured according to the initial control word, as required by claims 3 and 9. At no time does Wilson compare a frequency at either bound of the operating curve to the input frequency.

C. Dependent Claims 4 and 10

In claim 4, the logic circuitry determines the initial control word using fast comparisons between an actual frequency at the predetermined control voltage and the desired frequency and determines whether the initial control word should remain the same by using more precise comparisons between the actual frequency and the desired frequency. The Examiner contends that Nelson discloses fast comparisons when SW2 is closed and more precise comparisons take place with SW1 is closed, citing paragraph [0022]. However, paragraph [0022] of Nelson states that during *normal* operations, SW1 is closed and SW2 is open, the allowing loop-filter voltage V_{LF} to be applied to the VCO. There is no teaching that SW1 is used *to calibrate the voltage controlled oscillator to frequency range*, since it is not used during calibration.

D. Dependent Claims 5 and 11

In claims 5 and 11, the initial control word is tested by determining whether the difference between the desired frequency and an actual frequency for the voltage controlled oscillator while configured according to the initial control word is within a predetermined threshold. Paragraph [0018] of Nelson, cited by the Examiner as showing this element, has no such teaching. The Examiner states that the initial control word (L) is within a predetermined threshold (Max and Min). L, as used in paragraph [0018] of Nelson, denotes the range of control words which can be used to select an operating curve. Each operating curve has a minimum frequency (f_{MIN}) and maximum frequency (f_{MAX}). L cannot be "within a predetermined threshold (Max and Min)", because L is not a frequency. Paragraph [0018] does not talk about a desired frequency that can be compared to the minimum and maximum frequencies, nor does it discuss comparing a difference between a desired frequency and an actual frequency, nor does it compare a frequency difference with a threshold.

viii. Claims appendix

Listing of Claims:

1. A tuning circuit comprising:

a voltage controlled oscillator for generating a first clock signal comprising:

an inductive element;

a variable capacitive element coupled to the inductive element;

a bank of switched capacitors coupled to the inductive element and the variable capacitive element;

a frequency divider for generating a second clock signal responsive to the first clock signal and a selected divisor;

frequency control circuitry for adjusting a control voltage to the variable capacitive element responsive to a frequency difference between the second clock signal and a reference signal to oscillate the first clock signal at a desired frequency; and

logic circuitry for calibrating the voltage controlled oscillator to a frequency range inclusive of a new desired frequency responsive to a change in the divisor by:

performing a coarse search by operating the voltage controlled oscillator at a single predetermined control voltage for various capacitive settings of the bank to determine an initial control word for configuring the bank; and

testing the initial control word to determine whether the initial control word should be used to generate the first clock signal at the new desired frequency or whether the initial control word should be changed to an adjacent control word to generate the first clock signal at the new desired frequency.

2. The tuning circuit of claim 1 wherein said logic circuitry determines an initial control word to configure the bank by using a search having an accuracy that is greater than or equal to ±1 least significant bit of the initial control word.

3. The tuning circuit of claim 1 wherein the logic circuitry tests the initial control word by comparing the desired frequency to upper and lower bounds of a frequency range for the voltage controlled oscillator while configured according to the initial control word.

4. The tuning circuit of claim 3 wherein the logic circuitry determines the initial control word using fast comparisons between an actual frequency at the predetermined control voltage and the desired frequency and determines whether the initial control word should remain the same by using more precise comparisons between the actual frequency and the desired frequency.

5. The tuning circuit of claim 1 wherein the logic circuitry tests the initial control word by determining whether the difference between the desired frequency and an actual frequency for the voltage controlled oscillator while configured according to the initial control word is within a predetermined threshold.

6. The tuning circuit of claim 5 wherein an indication of the actual frequency is determined by counting clock cycles from the voltage controlled oscillator in a frequency divider circuit.

7. A method of calibrating a voltage controlled oscillator for generating a first clock signal, the voltage control oscillator having an LC tank with an inductive element, a variable capacitive element coupled to the inductive element, where the capacitance of the variable capacitive element is controlled by a control voltage, and a bank of switched capacitors coupled to the inductive element and the variable capacitive element, comprising the steps of:

determining an initial control word to configure the bank using a search in which the voltage controlled oscillator is operated at a single predetermined control voltage for various capacitive settings of the bank; and

testing the initial control word to determine whether the frequency range

produced by the initial control word should be used to generate the first clock signal at the new desired frequency or whether the initial control word should be changed to an adjacent control word to generate the first clock signal at the new desired frequency.

8. The method of claim 7 wherein said step of determining an initial control word comprises the step of determining an initial control word to configure the bank by using a search having an accuracy that is greater than or equal to ±1 least significant bit of the initial control word.

9. The method of claim 7 wherein the step of testing the initial control word comprises the step of comparing the desired frequency to upper and lower bounds of a frequency range for the voltage controlled oscillator while configured according to the initial control word.

10. The method of claim 9 wherein the step of determining the initial control word comprises the step of using fast comparisons between an actual frequency at the predetermined control voltage and the desired frequency and wherein the step of determining whether the initial control word should remain the same comprises the step of using more precise comparisons between the actual frequency and the desired frequency.

11. The method of claim 7 wherein the step of testing the initial control word comprises the step of determining whether the difference between the desired frequency and an actual frequency for the voltage controlled oscillator while configured according to the initial control word is within a predetermined threshold.

12. The method of claim 7 wherein the step of determining whether the difference between the desired frequency and an actual frequency is within a predetermined threshold comprises the step of calculating an indication of the actual frequency by counting clock cycles from the voltage controlled oscillator in a frequency divider circuit.

ix. Evidence appendix

None.

x. Related proceedings appendix

None.

xi. Conclusion

For the foregoing reasons, Appellants respectfully submit that the final rejection of claims 1 through 12 is in error. Reversal of the rejection is respectfully requested.

Respectfully submitted,

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